CLAIMS

What is claimed is:

Sub A1 A system for generating and storing trace bits for Viterbi decoding of binary convolution codes, the system comprising:

at least one arithmetic logic unit (ALU) for determining said trace bits; and

a first register and a second register for storing said trace bits.

2. A system according to claim 1 wherein said first register stores a first half of a series of trace bits for N states in sequential order and said second register stores a second half of said series in sequential order.

3. A system according to claim 2 wherein said first half comprises trace bits for states 0 to N/2–1 and said second half comprises trace bits for states N/2 to N–1.

4. A system according to claim 1 and wherein said at least one ALU is a first ALU and a second ALU and wherein said first register stores the trace bits determined by said first ALU and said second register stores the trace bits determined by said second ALU.

5. A system according to claim 1 and wherein said at least one ALU is one ALU operating in split mode.

6. A system according to claim 1 and wherein said first register and said second register are shift registers.

7. A system according to claim 1, the system further comprising:

at least one barrel shifter between said first register and one of said at least one ALU and between said second register and one of said at least one ALU.

8. A system according to claim 2, the system further comprising:

a storage device having memory cells, wherein a group of at least one memory cell stores said trace bits in sequential order.

9. A system according to claim 8 wherein each said group stores the trace bits for a stage.

10. A system according to claim 8 and wherein said group comprises one memory cell.

11. A system according to claim 10, the system further comprising:

means for packing said first half of said series of trace bits and said second half of said series of trace bits into said one memory cell so that said trace bits are packed sequentially in said memory cell.

12. A system according to claim 2, the system further comprising:

a storage device having groups of P memory cells, P being a power of 2 and P having a value of at least 2, said memory cells storing said trace bits in sequential order,

wherein in each of said groups, memory cells 0 to P/2-1 jointly store said first half of said series of trace bits and memory cells P/2 to P-1 jointly store said second half of said series.

13. A system according to claim 12 and wherein P is 2.

14. A system according to claim 12 and wherein P is 4.

15. A system according to claim 12 and wherein P is 8.

16. A system according to claim 12 and wherein P is 16.

17. A system according to claim 12 and wherein P is 32.

18. A system according to claim 12 and wherein P is 64.

19. A binary convolution decoder having multiple stages each having N states, the decoder comprising:

at least one arithmetic logic unit (ALU) for determining trace bits for each of said N states for each of said multiple stages;

a first register and a second register for storing trace bits of at least a portion of one stage;

a storage device having memory cells, wherein for each of said multiple stages, a group of at least one memory cell stores said N trace bits in sequential order; and

means for tracing back, stage by stage, through said memory cells using said trace bits.

20. A decoder according to claim 19, wherein each of said memory cells has a length of at least N bits and said means for tracing back is operative to trace back in as few as two cycles per stage.

21. A decoder according to claim 19, wherein N is 16, each of said memory cells has a length of at least 16 bits and said means for tracing back is operative to trace back in as few as two cycles per stage.

22. A decoder according to claim 19, wherein N is 32, each of said memory cells has a length of at least 32 bits and said means for tracing back is operative to trace back in as few as two cycles per stage.

23. A decoder according to claim 19, the decoder further comprising:

a trace back register whose L+P-1 least significant bits indicate the location in said group of a bit whose trace bit is to be saved into the least significant bit of the register after the register is shifted right one bit, said location comprising the bit number given by the L least

significant bits of the register and the memory cell whose number in said group is given by the value in the P-1 bits of the register immediately to the left of said L least significant bits.

24. A method for testing the value of a bit in a single instruction for a processor, the method comprising the step of:

testing the value of the bit in said memory cell whose bit number is given by the L least significant bits of a register, regardless of the content of the other bits of said register,

wherein L is the integer part of the logarithm to base 2 of the length of said memory cell.

25. A method according to claim 24, wherein said step of testing comprises the steps of:

if said value is 1, setting a flag to 1; and

if said value is 0, setting said flag to 0.

26. A method according to claim 24, wherein said step of testing comprises the steps of:

if said value is 1, setting a flag to 0; and

if said value is 0, setting said flag to 1.

27. A method for Viterbi decoding of binary convolution codes, the method comprising the steps of:

generating a series of trace bits; and

storing a first half of said series sequentially in a first register and a second half of said series sequentially in a second register.

28. A method according to claim 27, wherein said first half comprises trace bits for states 0 to N/2-1 and said second half comprises trace bits for states N/2 to N-1.

29. A method according to claim 27, the method further comprising the step of:

saving said trace bits in sequential order to a group of at least one memory cells.

30. A method according to claim 29, wherein said group comprises one memory cell.

31. A method according to claim 30, the method further comprising the step of:

packing said first half of said series of trace bits and said second half of said series into said one memory cell so that said trace bits are packed sequentially in said memory cell.

32. A method according to claim 27, the method further comprising the step of:

storing said trace bits in sequential order in groups of P memory cells, P being a power of 2 and P having a value of at least 2,

wherein in each of said groups, memory cells 0 to P/2-1 jointly store said first half of said series of trace bits and memory cells P/2 to P-1 jointly store said second half of said series.

33. A method according to claim 32 and wherein P is 2.

34. A method according to claim 32 and wherein P is 4.

35. A method according to claim 32 and wherein P is 8.

36. A method according to claim 32 and wherein P is 16.

37. A method according to claim 32 and wherein P is 32.

38. A method according to claim 32 and wherein P is 64.

39. A method for Viterbi decoding of binary convolution codes, the decoding involving multiple stages each having N states, the method comprising the steps of:

determining trace bits for each storing said trace bits for each of said N states for each of said multiple stages;

storing trace bits of at least a portion of one stage in a girst register and a second register;

for each of said multiple stages, storing said N trace bits in sequential order in a group of at least one memory cell; and

tracing back, stage by stage, through said memory cells using said trace bits.

40. A method according to claim 39, wherein each of said memory cells has a length of at least N bits and said step of tracing back is performed in as few as two cycles per stage.

41. A method according to claim 39, wherein N is 16, each of said memory cells has a length of at least 16 bits and said step of tracing back is performed in as few as two cycles per stage.

42. A method according to claim 39, wherein N is 32, each of said memory cells has a length of at least 32 bits and said step of tracing back is performed in as few as two cycles per stage.

43. A method according to claim 39, wherein said step of tracing back comprises for each stage the step of:

shifting a register right one bit;

saving into the least significant bit of said register the trace bit located in the memory cell whose number in said group is given by the value of the P-1 bits of said register immediately to the left of the L least significant bits of said register and located at the bit number given by said L least significant bits of said register.